INTER AND INTRI CONNECT TO INTERRUPT INPUTS OF THE CPU. RELOADROST(7:0) [0:7|VPUTDRV|7:0] OUTPUTENABLE ENCODEREXCEEDSMINSPEED RELOADRUST(7:0) EVENTVALUE(7:0) OUTPUTDRV(7:0) ROSTEVENT NETFORWARDCNTEN POSITIONCUE MAXPOSITION[11:0] OUTPUT_GENERATOR OUTPUTGENERATOR Thrertick PLSRESET PLSRESET SELOUTPUTFO PLSCLK PLSRESET SELECTEVENT POSITIONCUE PLSCLK POSITION(11:0] SETPOINT_EVENT SETPOINT_EVENT SPEEDCHECK PLSCLK MAXPOSITION[11:0] PLSCLK PLSRESET SELOUTPUT[7:0] SELECTEVENT NETFORWARDCNTEN POSITIONCUE ENCODER_POSITION_GENERATOR ENCODERPOSITIONGENERATOR MAXPOSITION(11:0] PHASEASIGN PHASEBSIGN INDEXSIGN USEINDEXEDGE PENCODERRESET PLSCLK FILTEROLK PHASEASIGN PHASEBSIGN INDEXSIGN USEINDEXEDGE MAXPOSITION(11:0) ENCODERRESET CLOCKGENERATOR CLOCK_GENERATOR

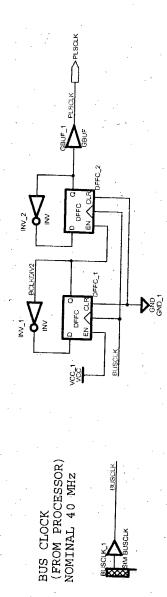
MAXROTATETIME[31:0]

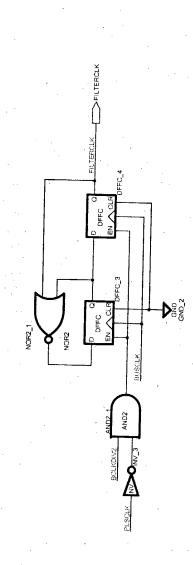
MAXROTATETIME(31:0

SPEED_CHECK

FIGURE 1 -- PROGRAMMABLE PULSE SEQUENCER

FIGURE 2 -- CLOCK GENERATOR





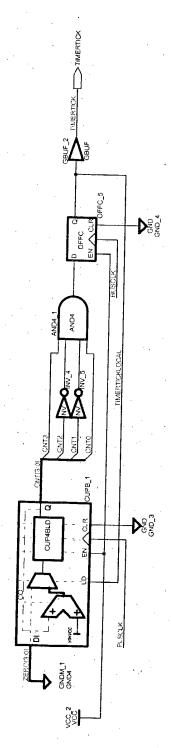
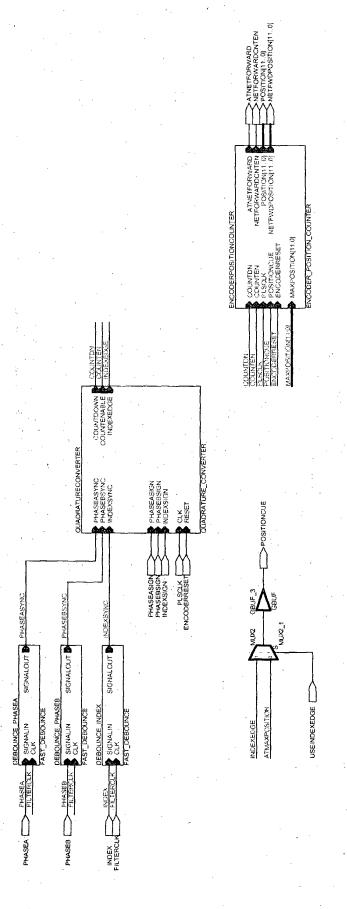
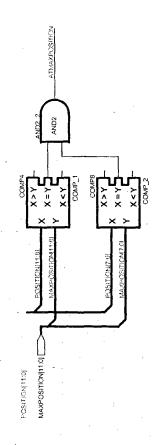


FIGURE 3 -- ENCODER POSITION GENERATOR

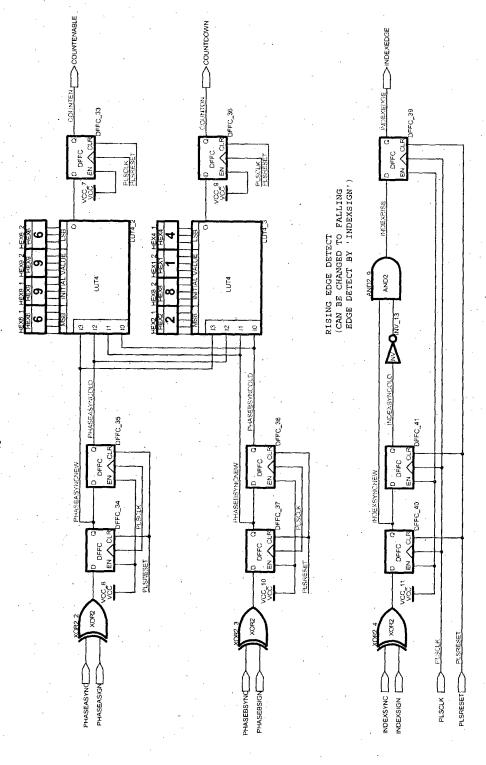




Da so D DFFC Q LUT4 5 G = D DFFC GEN Š 202

FIGURE 4 -- FAST SIGNAL DEBOUCE

FIGURE 5 -- QUADRATURE CONVERTER



NETFWDPOSITION[11.0] × ф AND2 12-BIT NET FORWARD POSITION REGISTER EN ACLR DFFCM_11 ACLR DFFCM_12 DFFCM_13 12-BIT POSITION REGISTER D DFFCA O D DFFC8 DFFC4 U DFFC8 NETFORWARDONTEN DFFS NXTPOSITION[11.0] MAXPOSITION[11:0] COUNTDN Ci ADDSUB_2 C. ADDSUB_3 12-BIT ADDSUB MAXPOSITION[11:0] POSITIONCUE JOIN4

-- ENCODER POSITION COUNTER WITH NET FORWARD POSTION REGISTER ဖ FIGURE

FIGURE 7 -- POSITION MULTIPLEXOR

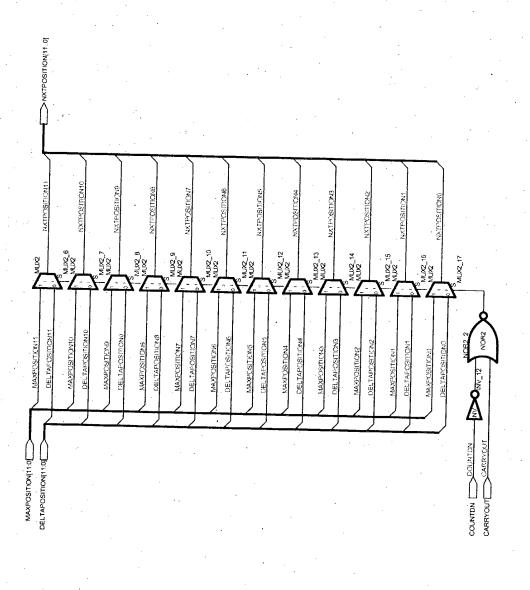


FIGURE 8 -- OUTPUT GENERATOR

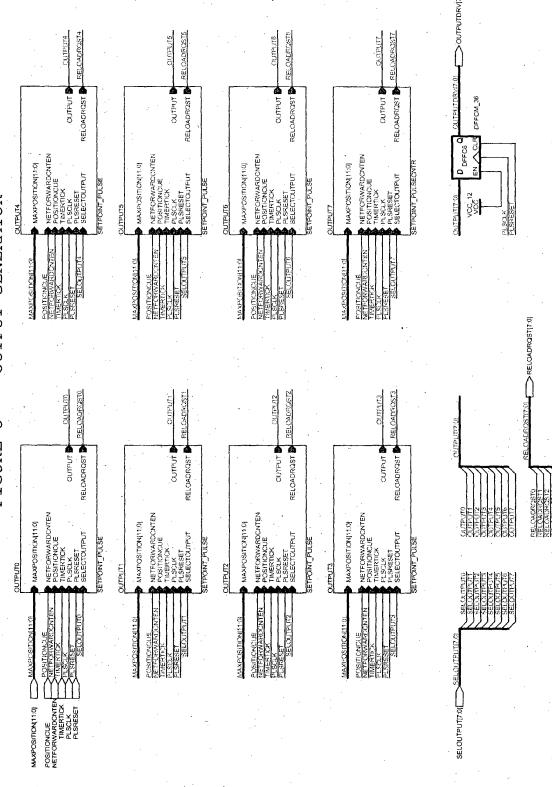
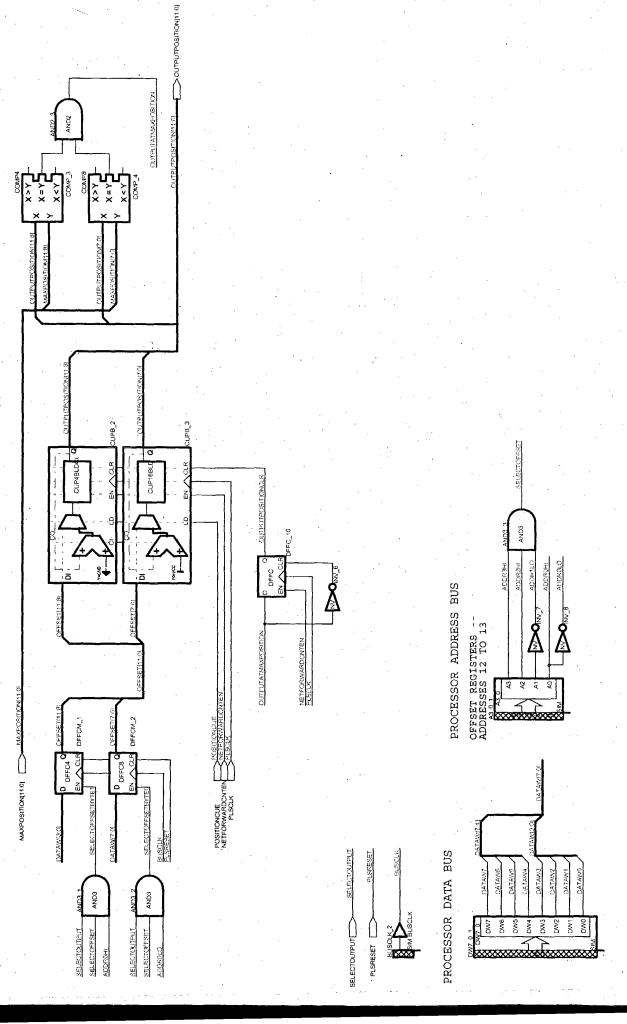


FIGURE 9 -- SETPOINT PULSE MODULE

FIGURE 10 -- OUTPUT POSITION COUNTER



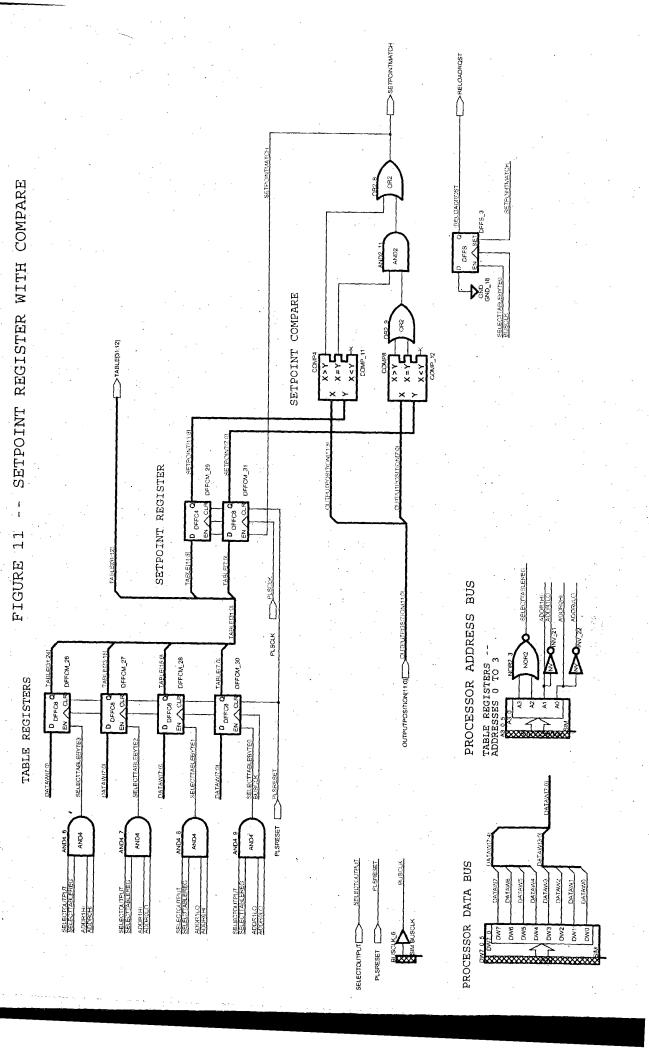
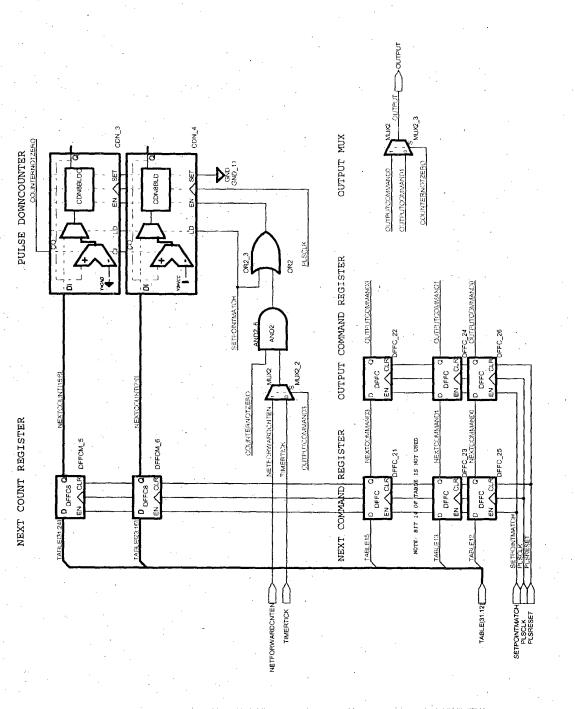
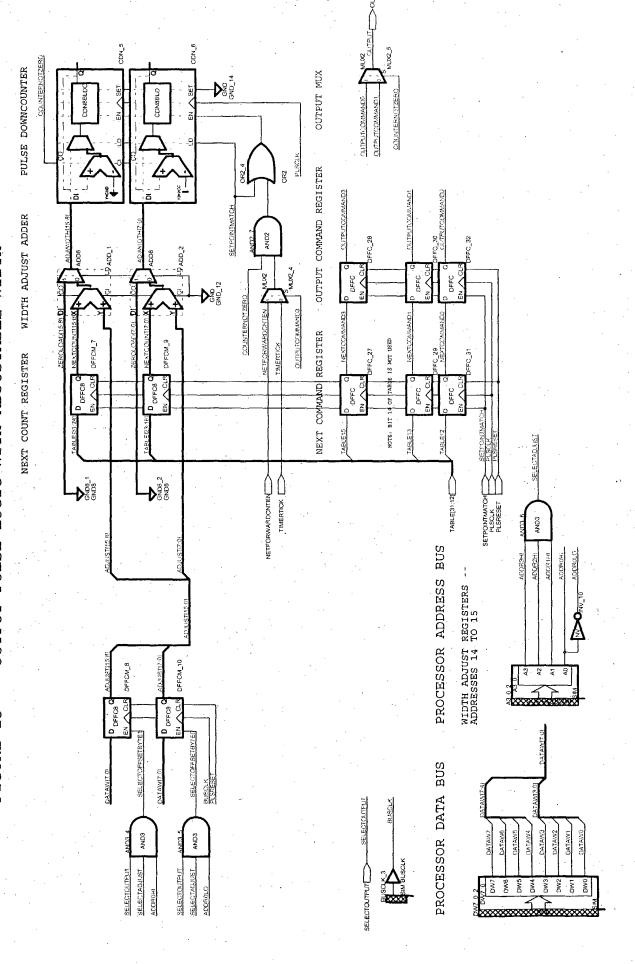


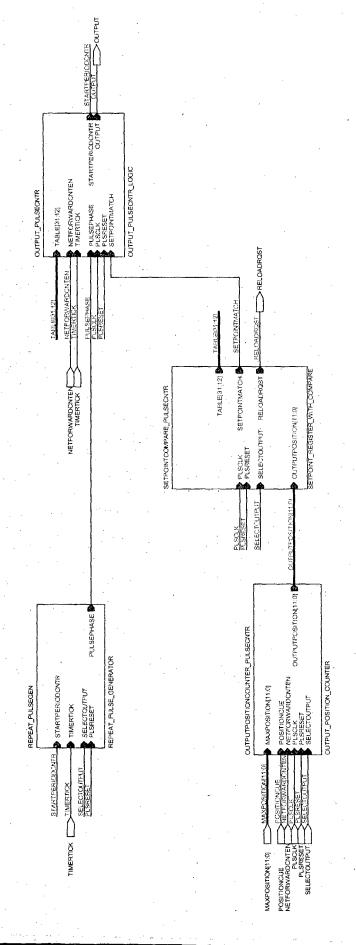
FIGURE 12 -- OUTPUT PULSE LOGIC



-- OUTPUT PULSE LOGIC WITH ADJUSTABLE WIDTH FIGURE 13



SETPOINT PULSE MODULE WITH OUTPUT PULSE COUNTER FIGURE 14



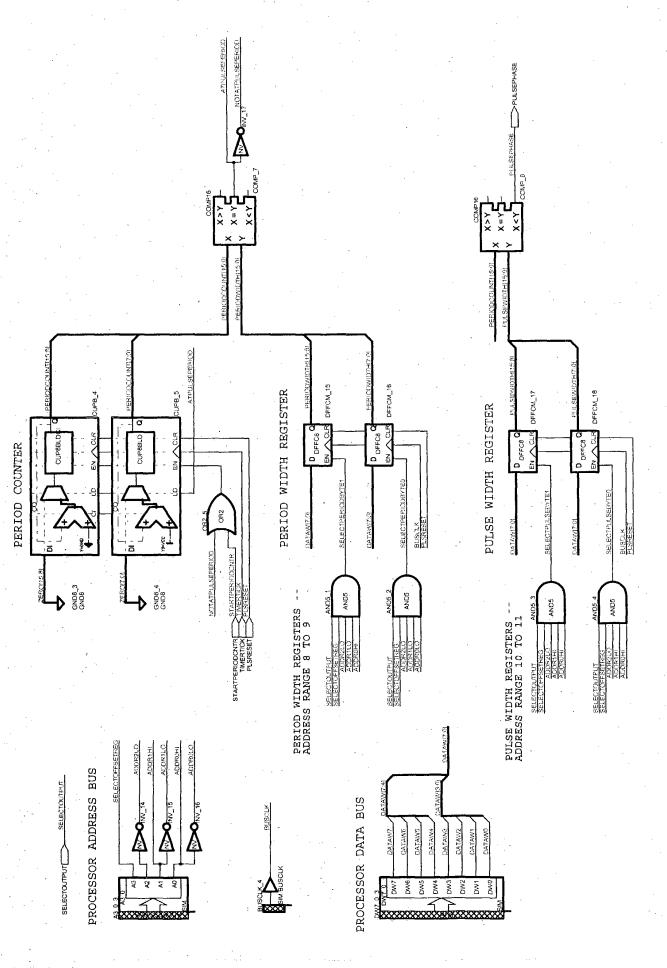


FIGURE 16 -- OUTPUT PULSE CNTR LOGIC

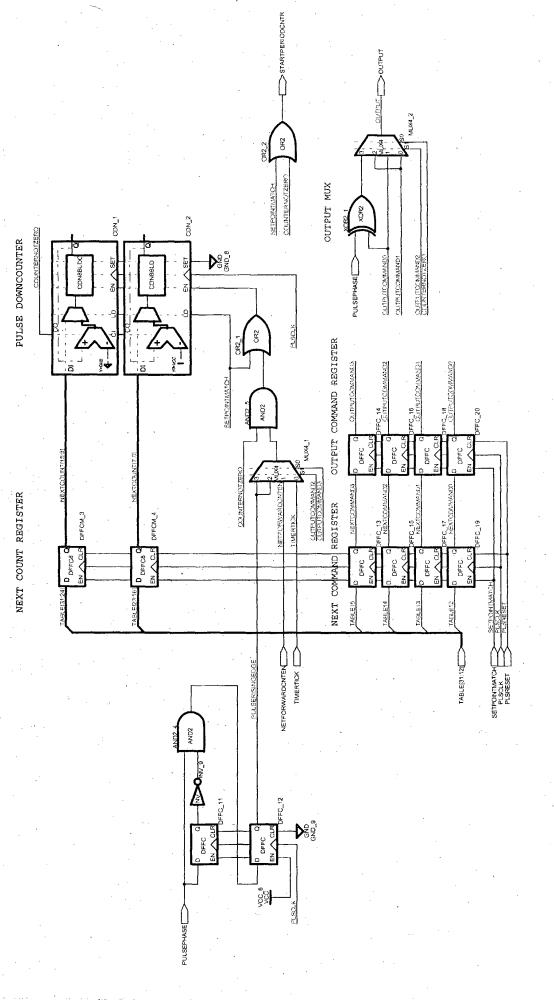
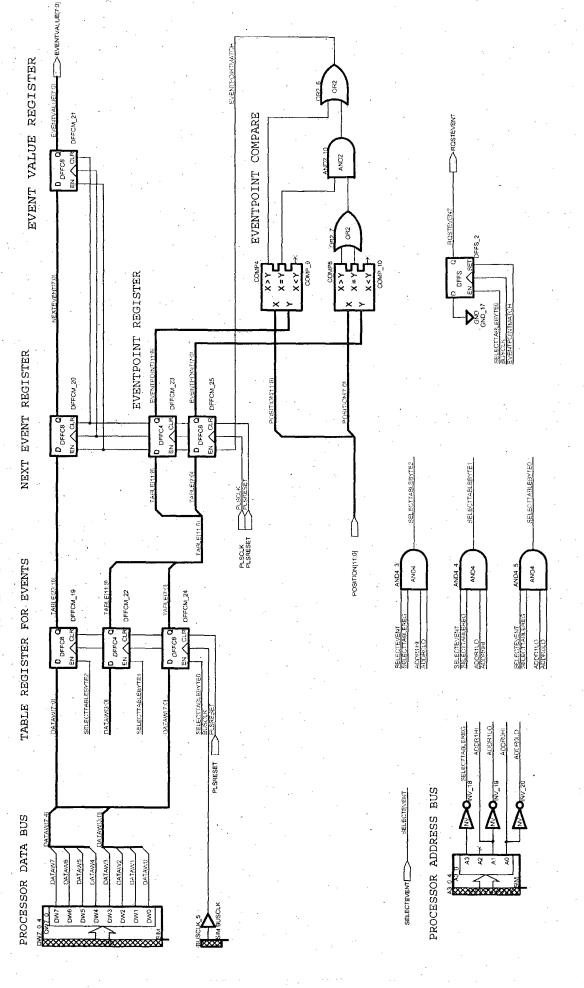


FIGURE 17 -- SET POINT EVENT



32-BIT ROTATION TIME COMPARE ROTATION TIME REGISTER DFFCM_33 DFFCM_34 D DFFC8 D DFFC8 D DFFC8 D DFFC8 CUPB_8 CUPB_7 CUPB_8 CUPB_9 GND_21 COUNTLIMIT D DFFC G POSITIONCUE PLSCLK MAXROTATETIME[31:0[

SPEED CHECK MODULE FIGURE 18 --

ROTATION COUNTER